In re Patent Application of:
ROCHE ET AL.
Serial No. **10/039,765**
Confirmation No. **9186**
Filed: **NOVEMBER 7, 2001**

REMARKS

In response to Decision on Appeal of May 13, 2010, the Applicants have now amended the independent claims to more clearly define the present invention over the cited prior art references. In addition, new claims have been added.

In particular, the independent claims have been amended to better illustrate that there is a double control of the line by which each device - a master or a slave - can be considered as a master as far as the duration of the clock period is concerned. Independent Claim 20 has been amended to include the subject matter from dependent Claims 21-23 and 25-26. Independent Claims 32 and 48 have been similarly amended. The remaining claims have been amended for consistency and/or cancelled.

The claims amendments and arguments supporting patentability of the claims are provided below.

I. The Claimed Invention

The present invention, as recited in independent Claim 20, for example, is directed to a method of transmitting data between a master device and a slave device via a clock line and at least one data line, with the clock line being maintained by default on a first logic value. The method comprises providing each master and slave device with the ability to tie the clock line to a potential representing a second logic value opposite the first logic value, and tying the clock line to the second logic value, via the master and slave devices, after data is applied to the data line. The tie to the clock line is

maintained by a first device of the master and slave devices to which the data is sent while the first device has not read the data. The data on the data line is maintained by a second device of the master and slave devices sending the data at least until an instant when the clock line is released by the second device to which the data is sent. The master device ties the clock line to the second logic value after applying data to the data line when the master device is sending the data to the slave device, and the slave device detects the second logic value on the clock line, then ties the clock line to the second logic value and reads the data, when the slave device is receiving the data from the master device. The master device ties the clock line to the second logic value when the master device receives data from the slave device, and the slave device detects the second logic value on the clock line, then ties the clock line to the second logic value, and applies the data to the data line, when the slave device is sending data to the master device.

The present invention may advantageously provide a double control of the line by which each device – a master or a slave – can be considered as a master as far as the duration of the clock period is concerned. This advantageously allows each device to impose its operating speed on the other, particularly in the event of disparity of clock frequencies or when one of the devices operates in multitasking on applications that have priority over the data transmission itself.

Independent Claim 32 has been amended similar to independent Claim 20.

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Independent Claim 48 has been amended similar to independent Claim 20.

II. The Claims Are Patentable

The Examiner rejected independent Claims 20, 32 and 48 over the SPI Block Guide in view of the System Management Bus (SMBus) Specification.

The Examiner has taken the position that FIG. 4-2 on page 27 in the SPI Block Guide illustrates that the clock line is maintained by default on a first logic value (SCK=1), and that one of the devices has the ability to tie the clock line to a potential representing a second logic value opposite the first logic value (SCK=0 at SCK Edge No. 1). The Examiner also characterized the SPI Block Guide as disclosing that the clock line is tied to the second logic value, via the two devices, after data is applied to the data line (data is applied before SCK Edge No. 1), and data on the data line is maintained by the device sending the data at least until an instant when the clock line is released by the device to which the data is sent (data is applied until rising edge of clock).

As correctly noted by the Examiner, the SPI Block Guide fails to disclose that the tie to the clock line is maintained by the device to which the data is sent while the device has not read the data. The Examiner cited the SMBus Specification as disclosing this feature. In particular, the Examiner referenced FIG. 4-7 on page 22 in section 4.3.3. The Examiner has taken the position that it would have been obvious to have the device

receiving data to hold the clock down, as disclosed by the SMBus Specification, in the method disclosed by the SPI Block Guide since this would allow clock synchronization so that slower slave devices could interface with faster masters.

The Applicants submit that even if the references were selectively combined as suggested by the Examiner, the claimed invention is still not provided.

A. Interpretation of Independent Claims 20 and 32

Claim 20 relates to a method of transmitting data between two devices via a clock line and at least one data line.

Claim 32 relates to a method of transmitting data between two devices connected via a clock line and at least one data line.

The method according to Claims 20, 32 comprises the five following features (which are defined below using the language of the claims):

Feature F1
- The clock line is maintained by default on a first logic value (Claim 20).
- Maintaining the clock line on a first logic value as a default (Claim 32).

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Feature F1 means that the clock line is polarized by a static component, such as a pull-up resistor (the first logic value being "1" in this case). This is illustrated in FIG. 1 of the application, representing the two devices D1 and D2:

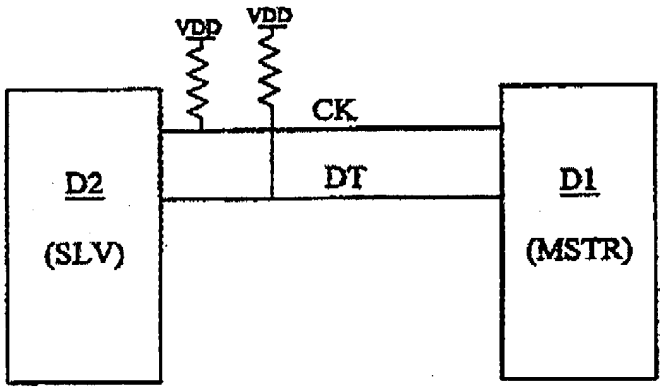

FIG. 1

The first logic value, or default logic value, is generally 1 when a pull-up resistor is used.

Feature F2
- Each device has the ability to tie the clock line to a potential representing a second logic value opposite the first logic value (Claim 20).
- Providing each device with the ability to tie the clock line to a potential representing a second logic value (Claim 32).

Feature F2 means that the control of the clock value is under control of both devices, i.e., both can tie the clock at the same time.

Features F1 and F2 imply that the control of the clock is in practice implemented by means of the "open drain" technique, which includes tying the clock line to ground by turning ON a transistor when the clock signal must be set to 0, and turning OFF the transistor so as to release the clock line when the clock signal must be set to 1 (when the default logic value is 1).

The terms "maintained by default"; "tying", and "releasing" were intentionally chosen by the Applicants to evoke the open-drain technique, and the fact that the clock line returns to the default value when it is released.

Feature F3
- The clock line is tied to the second logic value, via the two devices, after data is applied to the data line (Claim 20).
- Tying the clock line to the second logic value, via the two devices, after data is applied to the data line (Claim 32).

Feature F4

- The tie of the clock line is maintained by the device to which the data is sent while the device has not read the data (Claim 20).
- Maintaining the tie to the clock line by the device to which the data is sent while the device has not read the data (Claim 32).

Feature F5
- The data is maintained on the data line by the device sending the data at least until an instant when the clock line is released by the device to which the data is sent (Claim 20).
- Maintaining the data on the data line by the device sending the data at least until the clock line is released by the device to which the data is sent (Claim 32).

Feature F3 means that there is at least one instant during which the two devices tie the clock to the second logic value, after a data has been applied to the data line. Features F3, F4 is to be interpreted together and in combination with feature F3. According to feature F3, there is at least one instant during which the two devices tie the clock to the second logic value. This implies that the invention may be implemented in two ways:

Case 1: The device that sends the data is the first to tie the clock line, or

Case 2: The device that reads the data is the first to tie the clock line.

A theoretical Case 3 also exists in which the two devices tie the clock line at the same time. However, in practice, this case is impossible to implement for synchronization reasons, or else does not make sense since it would necessitate a third line to synchronize the devices. In such a case, the other features of Claims 20/32 would have no interest since they aim to synchronize the devices. 4

These two possibilities thus define two possible interpretations (or implementations) of Claims 20/32.

Case #1 - the device that sends the data is the first to tie the clock line

In this embodiment, the method contains the following features:

- Feature P1: the device that sends the data indicates to the other device that the data is available on the data line by tying the clock line (basic hypothesis).
- Feature P2: the other device must then also tie the clock line (implicit: results from P1 and feature F3).
- Feature P3: the device that reads the data indicates to the other device that it has read the data by releasing the clock line (explicit: feature F4).

- Feature P4: the device that sends the data maintains the data until it knows that the other device has read the data, i.e. until the other device has released the clock line (explicit: feature F5).

Case #1 is, for example, shown in FIG. 3A of the application:

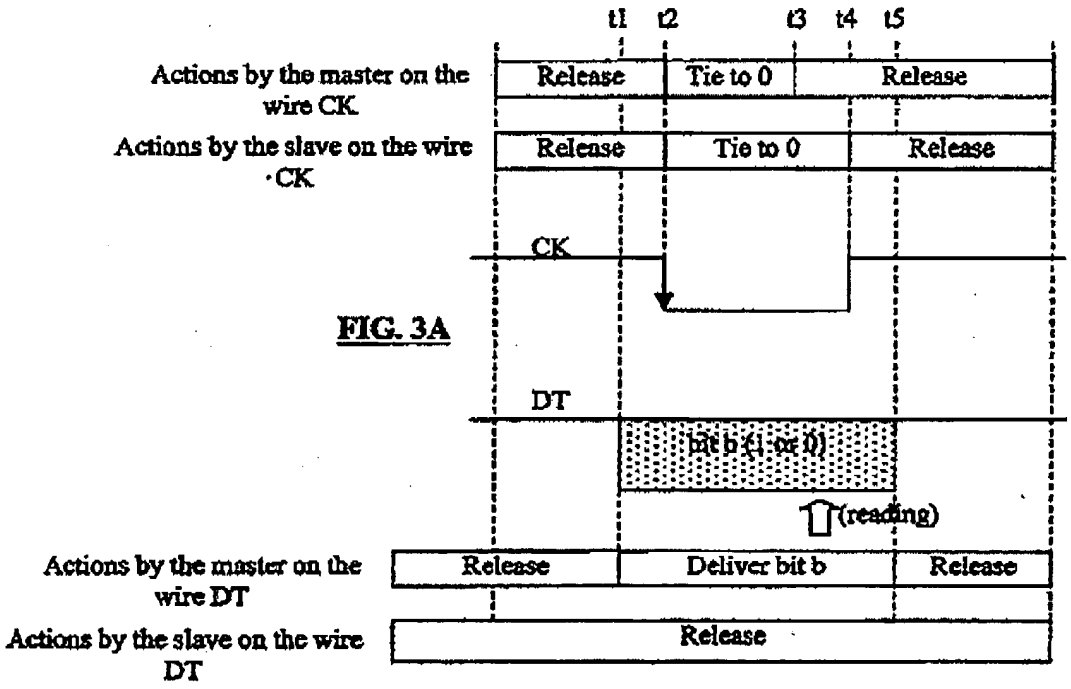

FIG. 3A

It can be noted that the device that sends the data is not necessarily the first to release the clock line; it can perform data processing, then release the clock line, and then

check whether the other device has released the clock line since feature F5 consists of "maintaining the data on the data line by the device sending the data at least until the clock line is released by the device to which the data is sent". This is illustrated in FIG. 3B.

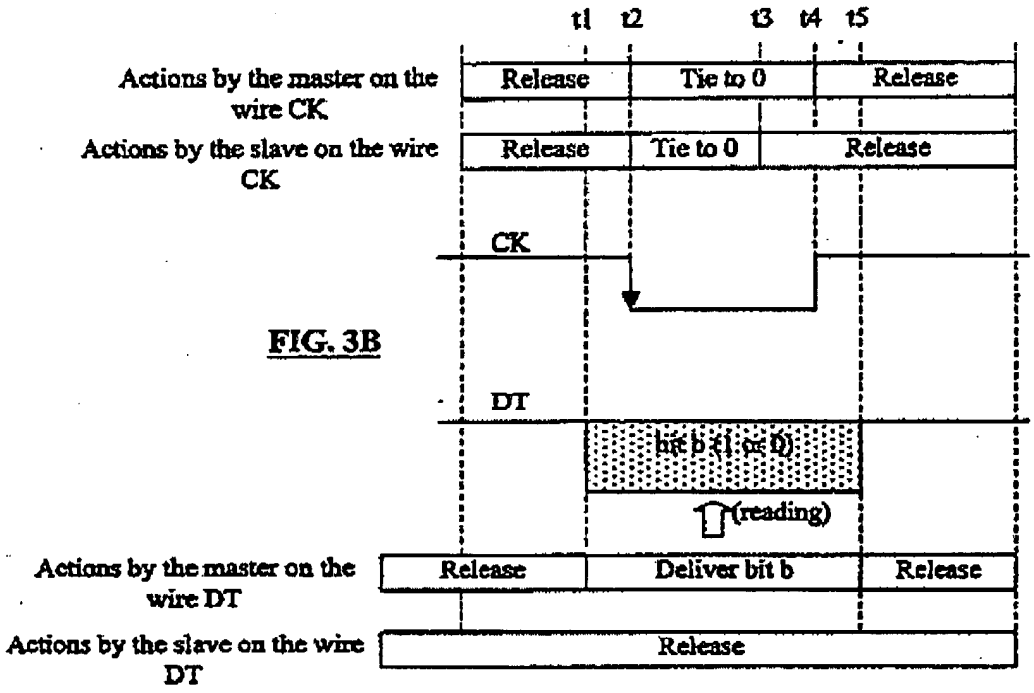

FIG. 3B

It can also be noted that features P1 and are explicitly defined in Claims 21, 22, and 23, the subject matter of which has now been included in independent Claims 20, 32:

- Claim 21 specifies that one of the two devices is a master device and the other is a slave device, and that the master device ties the clock line to the second logic value before the slave device when data is transmitted, regardless of the direction in which the data is transmitted.

- Claim 22 specifies that the master device ties the clock line to the second logic value after applying data to the data line when the master device is sending the data to the slave device.

- Claim 23 specifies that the slave device detects the second logic value on the clock line, then ties the clock line to the second logic value and reads the data when the slave device is receiving the data from the master device.

Case #2- the device that reads the data is the first to tie the clock line

This embodiment contains the following features:

- Feature P1': a device indicates to the other device that it is ready to read the data by tying the clock line (basic hypothesis).
- Feature P2': the other device must detect that the clock line has been tied, then apply the data to the data line (results from P1' and feature F2) and also tie the clock line (implicit: results from P1' and feature F3).

- Feature P3: the device that read the data indicates to the other device that it has read the data by releasing the clock line (explicit: feature F4).
- Feature P4: the device that sends the data maintains the data until it knows that the other device has read the data, i.e., until the other device has released the clock line (explicit: feature F5).

This method is, for example, shown in FIG. 5B of the application:

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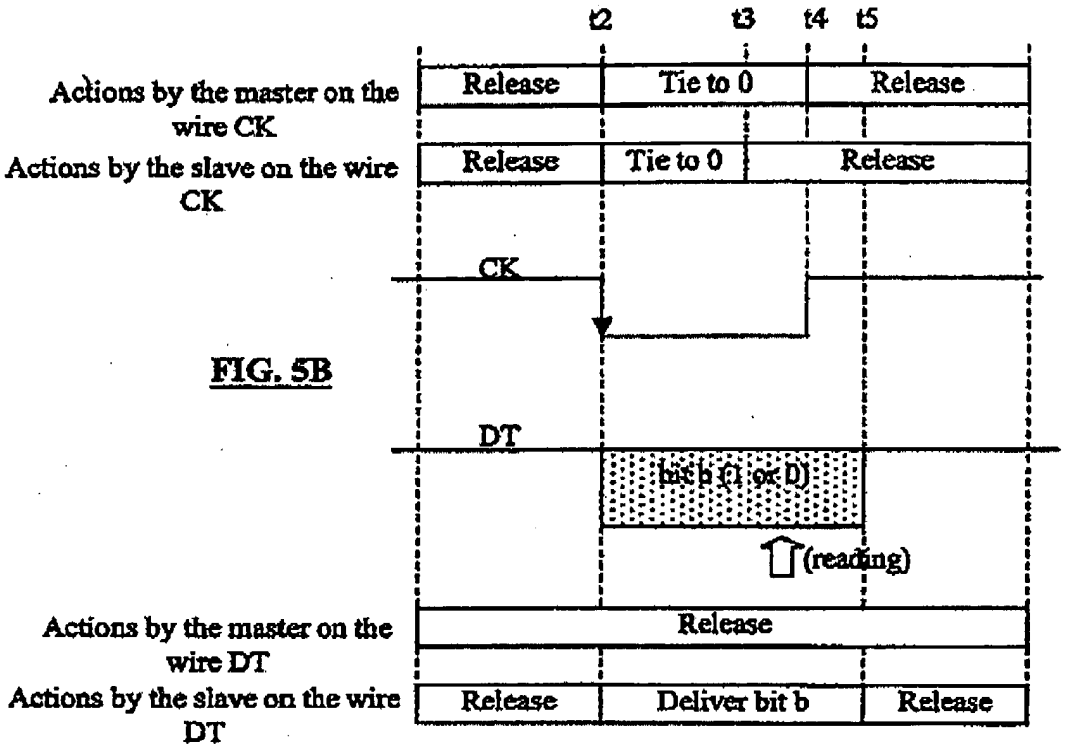

FIG. 5B

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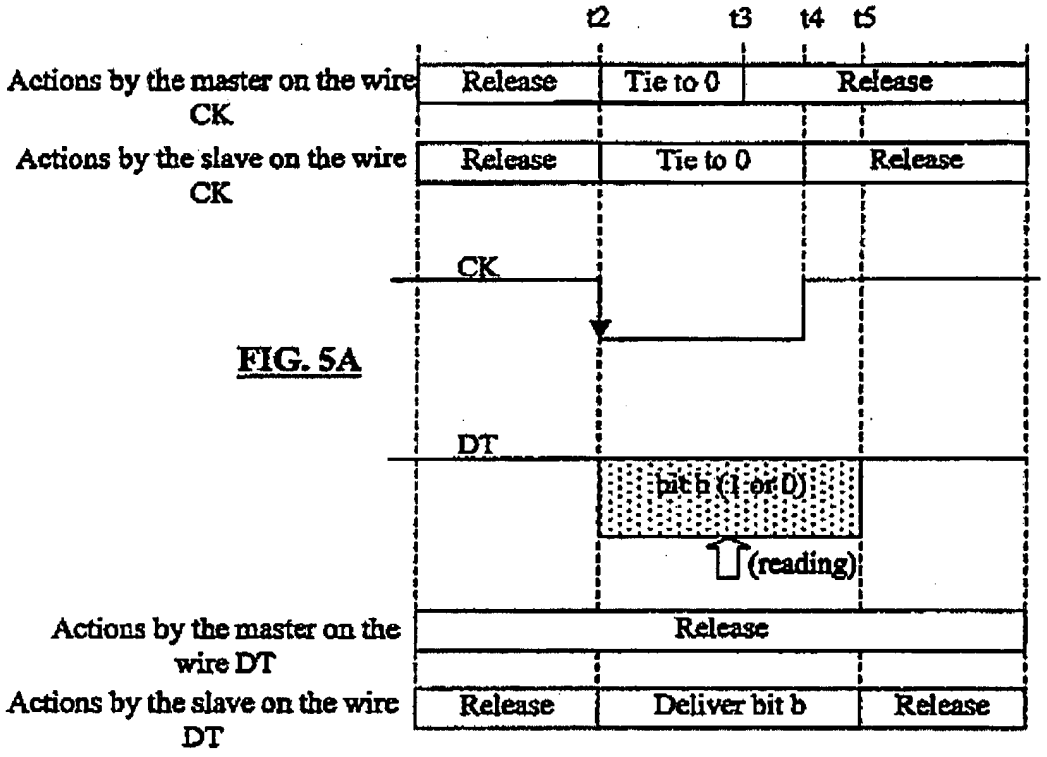

FIG. 5A

It can again be noted that the device that sends the data is not necessarily the first to release the clock line; it can perform data processing, then release the clock line, and then check whether the other device has released the clock line since feature F5 consist of "maintaining the data on the data line by the device sending the data at least until the clock line is released by the device to which the data is sent." This is also described in FIG. 5A.

It can also be noted that features P1' and P2' are explicitly defined in Claims 21, 25, and 26, the subject matter of which has now been included in independent Claims 20 and 32.

- Claim 21 specifies that one of the two devices is a master device and the other is a slave device, and that the master device ties the clock line to the second logic value before the slave device when data is transmitted, regardless of the direction in which the data is transmitted.

- Claim 25 specifies that the master device ties the clock line to the second logic value when the master receives data from the slave device.

- Claim 26 specifies that the slave device detects the second logic value on the clock line, then ties the clock line to the second logic value, and applies the data to the data line when the slave device is sending data to the master device.

B. Summary of the Scope of Independent Claims 20 and 32

The invention can be defined as a sort of handshake technique using a signal called "clock signal" as a handshake signal. Handshake is defined in the literature as "The interchange of signals between a 'talker' and a 'listener' to exchange data on a bus. In data communications, a sequence of events governed by hardware or software, requiring mutual agreement of the state of the operational modes prior to information exchange."

The originality of the invention is that this handshake technique is implemented by way of a technique of a mutual tying of a line having a default value, called a "clock line" in the application. However, there is no real "clock" in the invention, and another language may have been used by the inventors but became lost in the translation from the French priority patent application. A clock is a periodic signal which is controlled by the device that issues it.

In the invention, the falling edge of the clock is controlled by one and only one device (except the hypothetic Case 3 evoked above), whereas the rising edge is controlled by the two

devices. Perhaps this signal should have been called something other than "clock", such as "acknowledgement signal", since its function is:

- to allow the device which ties it the first to say "a data is ready to be read" (Case 1) or "I want to read a data" (Case 2).
- to allow the device which read the data to say "it is OK, I have read the data, you can release the data line".

In fact, if the term "clock" had not been used, it is likely that the Examiner would not have used the current references to reject the application.

To summarize, the claimed invention defines a line called "clock line" on which there is a signal called "clock", which is actually a handshake signal and whose essential function is to allow two devices to exchange three types of handshake messages:

Message M1- "a data is ready to be read", or
Message M2- "I want to read a data", and
Message M3 - "It's OK I have read the data, you can release it".

The method of transmitting data as defined by Claims 20, 32 also contains the implicit feature that a data is read when the handshaking signal has a logic value opposite that of the default logic value, since Claims 20, 32 states that "the tie

of the clock line is maintained by the device to which the data is sent while the device has not read the data" (feature F4) and "data is maintained on the data line by the device sending the data at least until an instant when the clock line is released by the device to which the data is sent" (feature F5).

C. Prior Art Reference: SPI

1. General teaching

SPI describes a bus having a clock line SCK and two data lines MOSI (Master Output, Slave Input) and MISO (Master Input, Slave Output). A block diagram is shown on page 13, and is provided below.

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Figure 1-1 gives an overview on the SPI architecture. The main parts of the SPI are status,control and data registers, shifter logic, baud rate generator, master/slave control logic and port control logic.

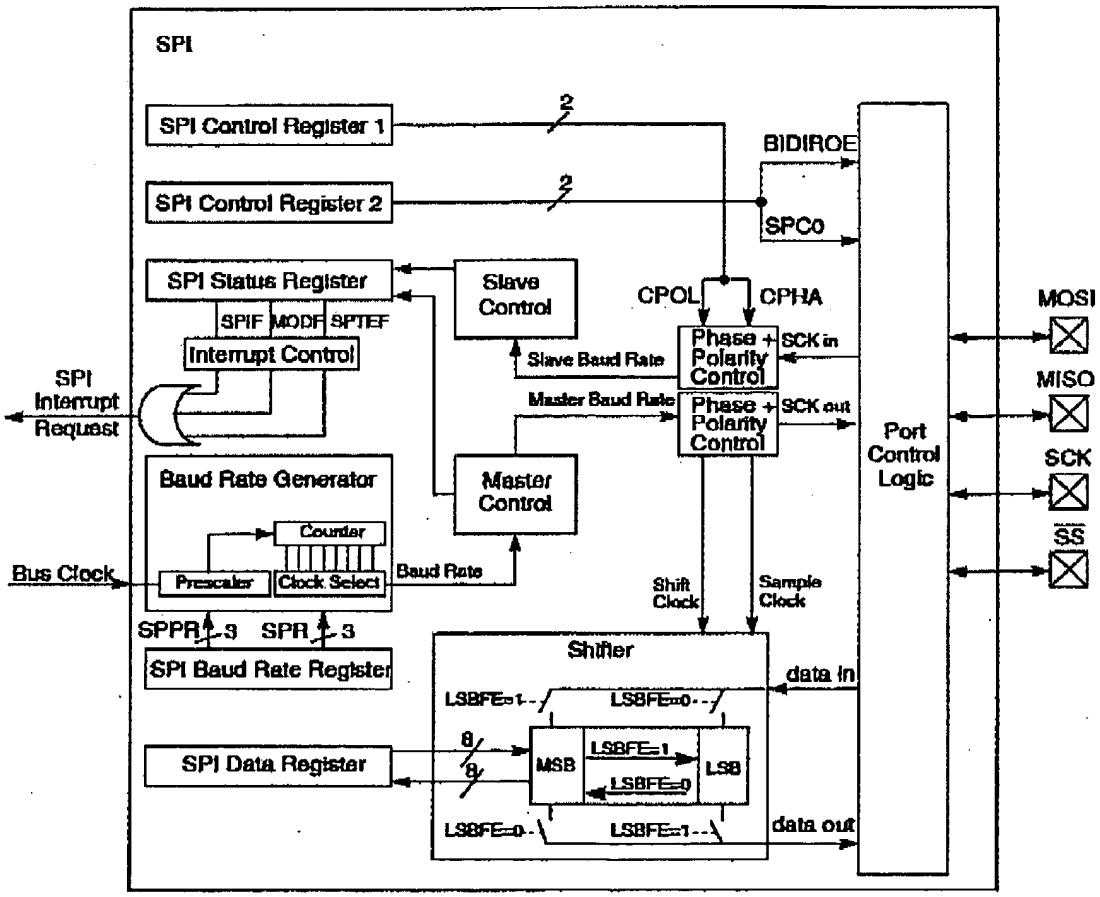

Figure 1-1 SPI Block Diagram

The polarity and the phase of the clock are respectively controlled by a clock polarity bit CPOL and a clock phase bit CPHA.

- CPOL defines the idle value of the clock, i.e. if CPOL=1 the idle value is 1 and if CPOL=0 the idle value is 0.
- CPHA defines the edge of the clock (even or odd) on which the data are sampled.

Cf. Page 17:
CPOL – SPI Clock Polarity Bit

This bit selects an inverted or non-inverted SPI clock. To transmit data between SPI modules, the SPI modules must have identical CPOL values. In master mode, a change of this bit will abort a transmission in progress and force the SPI system into idle state.

1 = Active-low clocks selected. In idle state SCK is high.
0 = Active-high clocks selected. In idle state SCK is low.

CPHA – SPI Clock Phase Bit

This bit is used to select the SPI clock format. In master mode, a change of this bit will abort a transmission in progress and force the SPI system into idle state.

1 = Sampling of data occurs at even edges (2,4,6,...,16) of the SCK clock

0 = Sampling of data occurs at odd edges (1,3,5,...,15) of the SCK clock

Cf. also page 25:

If the CPHA bit in SPI Control Register 1 is clear, odd numbered edges on the SCK input cause the data at the serial data input pin to be latched. Even numbered edges cause the value previously latched from the serial data input pin to shift into the LSB or MSB of the SPI shift register, depending on the LSBFE bit.

If the CPHA bit is set, even numbered edges on the SCK input cause the data at the serial data input pin to be latched. Odd numbered edges cause the value previously latched from the serial data input pin to shift into the LSB or MSB of the SPI shift register, depending on the LSBFE bit.

When CPHA is set, the first edge is used to get the first data bit onto the serial data output pin. When CPHA is clear and the SS input is low (slave selected), the first bit of the SPI data is driven out of the serial data output pin. After the eighth shift, the transfer is considered complete and the received data is transferred into the SPI Data Register. To indicate transfer is complete, the SPIF flag in the SPI Status Register is set.

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2. In summary, SPI objectively discloses the following:

SPI discloses a bus upon which data are latched during one edge of a clock signal and are refreshed (changed) during the other edge of the clock signal. The clock has an active value and an idle value. A bit CPOL defines the active value and the idle value of the clock. A bit CPHA defines which edge of the clock is used to sample the data.

The teaching of SPI is summarized by the figures below.

In FIG. 4-2, CPHA=0 and
- The data are latched at the edge of the clock when the clock goes from the idle value (1 if CPOL=1 or 0 if CPOL=0) to the active value;
- The data are refreshed at the edge of the clock when the clock goes back to the idle value.

In FIG. 4-3, CPHA=1 and
- The data are refreshed at the edge of the clock when the clock goes from the idle value (1 if CPOL=1 or 0 if CPOL=0) to the active value;
- The data are latched at the edge of the clock when the clock goes back to the idle value.

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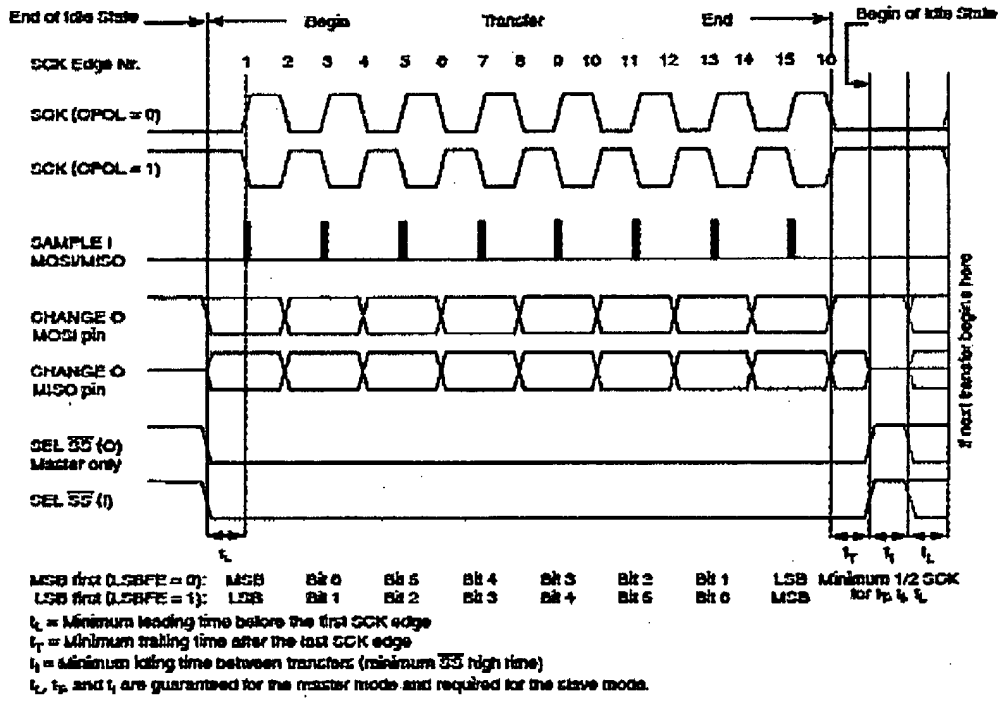

Figure 4-2 SPI Clock Format 0 (CPHA = 0)

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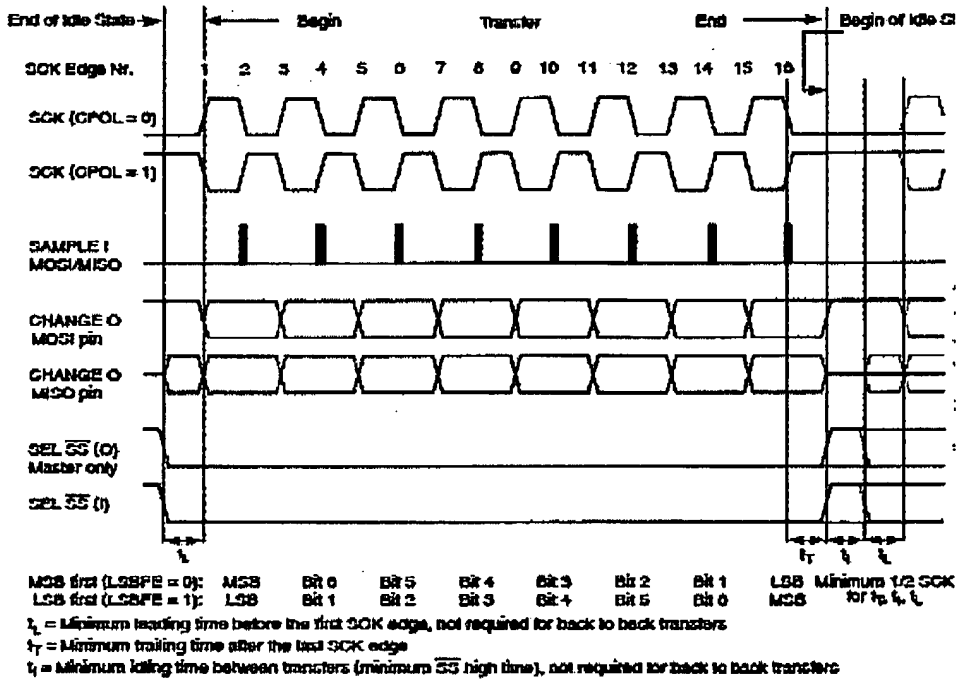

Figure 4-3 SPI Clock Format 1 (CPHA = 1)

D. Prior Art Reference: SMB Specification

1 - General teaching

The SMB specification discloses a bus using open-drain lines with pull-up polarization (first default logic value) and pull-down control for sending a clock signal and data.

The SMB bus has one open-drain data line SMBDAT and one open-drain clock line SMBCLK, see for example page 9 FIG. 2-1, page 10 Figs. 2-2 and 2-3.

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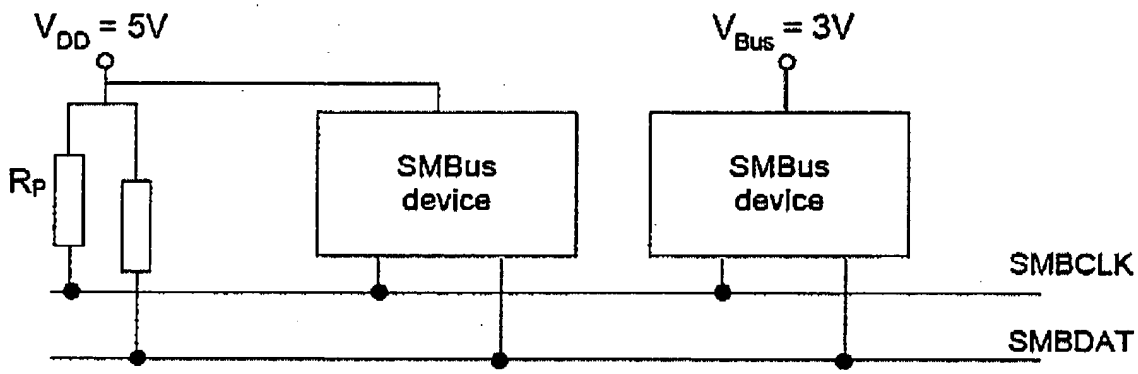

Figure 2-1: SMBus Topology

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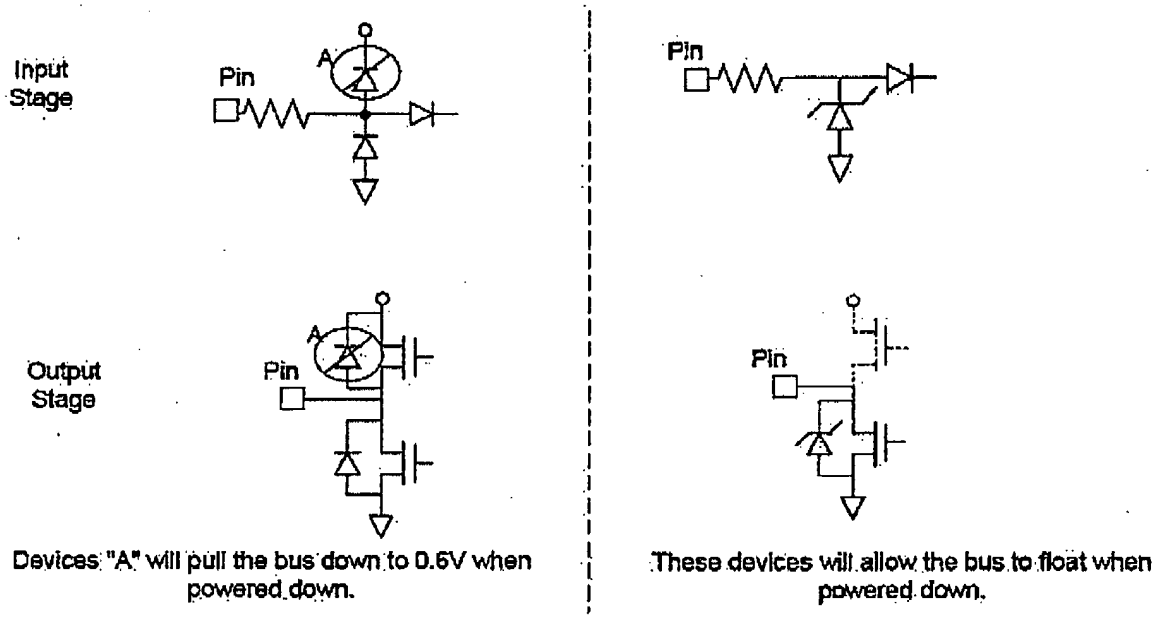

Figure 2-2: Example input and output stages of SMBus devices

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Citation:

"A device that wants to place a 'zero' on the bus must drive the bus line to the defined logic low voltage level. In order to place a logic 'one' on the bus the device should release the bus line letting it be pulled high by the bus pull-up circuitry."

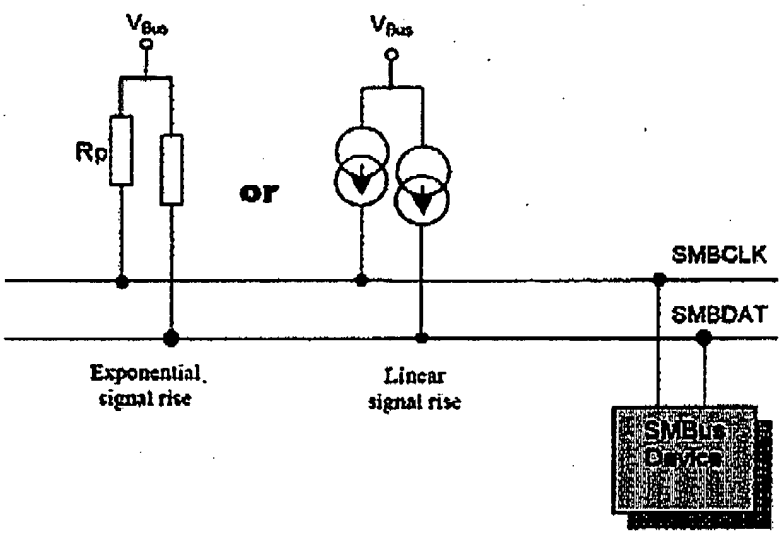

Figure 2-3: SMBus pull-up circuitry

"The bus lines may be pulled high by a pull-up resistor or by a current source. In cases that involve higher bus capacitance, a more sophisticated circuit may be used that can limit the pull-down sink current while also providing enough current during the low-to-high transition to maintain the rise time specifications of the SMBus."

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On page 18, paragraph 4.1, it is indicated that data are valid when CLK is high (the default logic value) and data can be changed ("change of data allowed") when CLK is low.

4.1.1. Data validity

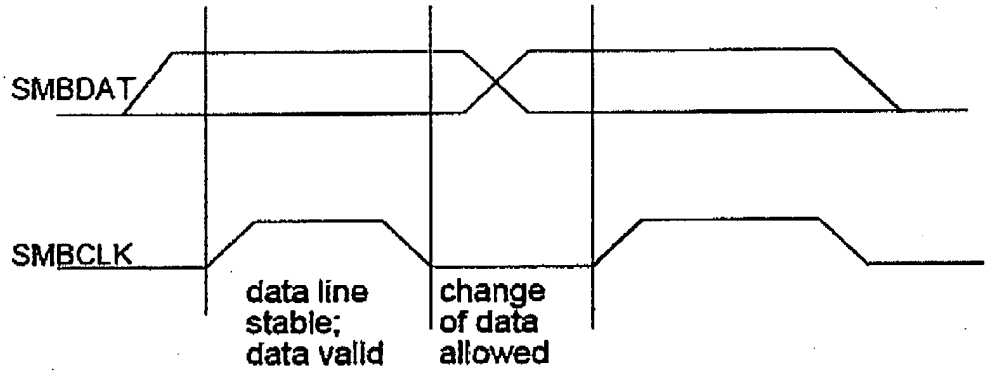

Figure 4-1: Data validity

On page 19, paragraph 4.2 and FIG. 4-3, it is also shown that the change of data on the SMBDAT line is performed when the SMBCLK line is low, see for example, FIG. 4-3.

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4.2. Data transfers on SMBus

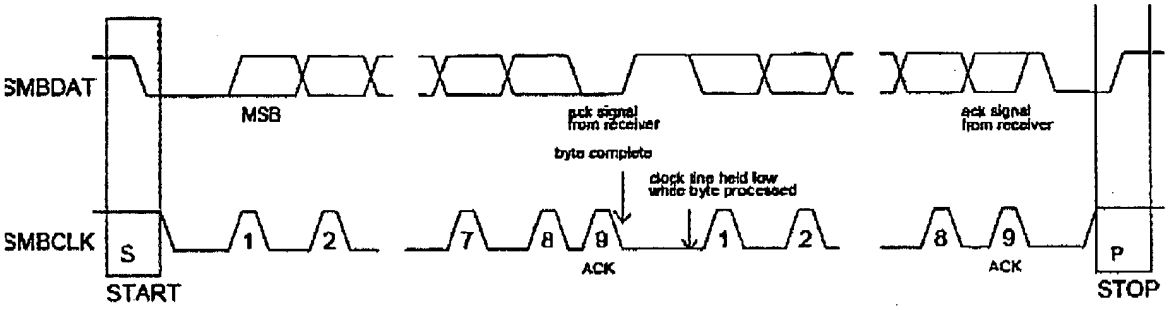

Figure 4-3: SMBus byte format

2 – Particular teaching

On page 22 and FIGS. 4-7, 4-8 is disclosed an information called "clock low extending."

It is indicated, on pages 22 and 23:

4.3.3. Clock low extending

SMBus provides a clock synchronization mechanism to allow devices of different speeds to co-exist on the bus. In addition to the bus arbitration procedure the clock synchronization mechanism can be used during a bit or a byte transfer in order to allow slower slave devices to cope with faster masters.

At the bit level, a device may slow down the bus by periodically extending the clock low interval.

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Devices are allowed to stretch the clock during the transfer of one message up to the maximum limits described in the AC specifications of this document. Nevertheless, devices designed to stretch every clock cycle periodically must maintain the fSMB,MIN frequency of 10 KHz (fSMB,MIN -1= 100µs) in order to preserve the SMBus bandwidth.

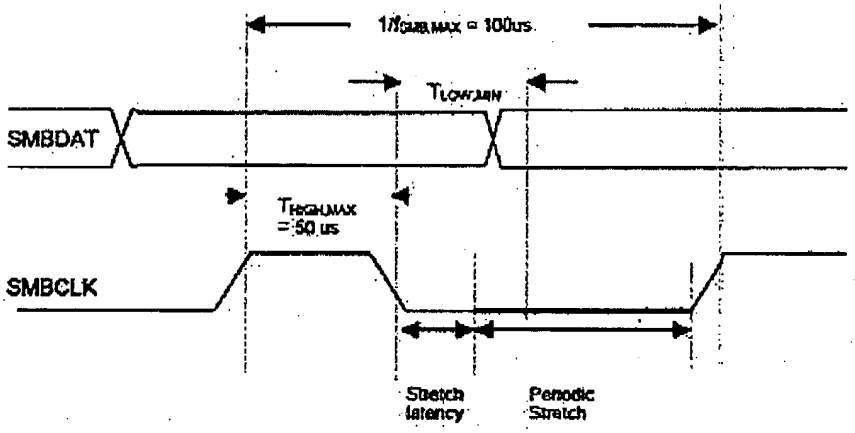

Figure 4-7: Periodic clock stretching by a slave SMBus device

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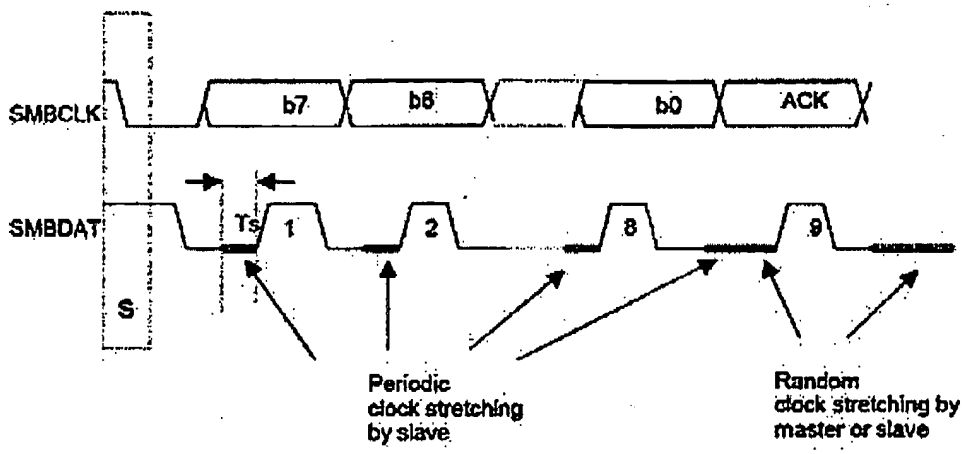

Figure 4-8: Periodic and random clock stretching

Clock LOW extension, or stretching, if necessary, must start after the SMBCLK high-to-low transition within a TLOW:MIN - TSU:DAT interval. Devices designed to stretch the clock on every bit transfer must maintain the minimum bus frequency fSMB,MIN of 10 KHz. A slave device may opt to stretch the clock line during a specific bit transfer in order to process a real time task or check the validity of a byte. In this case the slave device must adhere to the TTIMEOUT and TLOW:SEXT specifications. Clock LOW extension may occur during any bit transfer including the clock provided prior to the ACK clock pulse.

A slave device may select to stretch the clock LOW period between byte transfers on the bus, in order to process received data or prepare data for transmission. In this case the

slave device will hold the clock line LOW after the reception and acknowledgement of a byte. Again the slave device is responsible for not violating the TLOW:SEXT specification of SMBus.

During a bus transaction the master also can select to extend the clock LOW period between bytes or at any point in the byte transfer, including the clock LOW period after the byte transfer and before the acknowledgement clock. The master may need to extend the clock LOW period selectively in order to process data or serve a real time task. In doing so, the master must not exceed the TLOW:MEXT specification

3. In summary, SMB objectively discloses the following:

SMB provides that a slave device may stretch the clock period (i.e., tie the clock line) when the clock signal is LOW, that is, to say outside the period of data validity (see FIG. 4.1.1 and FIG. 4.7 above), in other words within the period when the change of data is allowed.

In the invention, the stretching of the clock is performed during the period when the data is valid, and allows the device to have more time to read the data, and then release the clock line to allow another bit to be sent on the data line.

According to SMB, the tie of the clock by the slave is provided after a data has been read, to delay the next read

phase, which will take place when the clock signal SMBCLK is again in the idle state. This is expressly indicated:

A slave device may opt to stretch the clock line during a specific bit transfer in order to process a real time task or check the validity of a byte.

This means that the slave device has already read the bit and needs time to check its validity.

Stretching the clock within or outside the period when the data are valid is not equivalent:

i) In the invention, as seen above, the release of the clock line means:

Message M3: "It's OK I have read the data, you can release it".
and the tie of the clock line means:

Message M1: "a data is ready to be read" (Case 1), or
Message M2: "I want to receive a data" (Case 2).

ii) In SMB, since the stretching of the clock occurs after the data has been read, it merely means

"I want to postpone the next data reading period".

In addition, Case 2 (where tying the clock line means "I want to receive a data" and is immediately followed by the tying of the clock line by the other device) does not exist in SMB.

E. - The Examiner's rejection arguments

The Applicants will now briefly comment upon the Examiner's arguments.

Argument 1: SPI discloses a method of transmitting data between two devices via a clock line and at least one data line, the clock line being maintained by default on a first logic value (SCK=1) , ... (see "argument 2")

Applicants' comment: "Default value" and "tying the clock line" need to be interpreted as referring to an open-drain technique with a polarization device such as a pull-up resistor. The Examiner has considered that the idle value defined by the polarization bit CPOL is equivalent to the default value of claim 1. However, this does not take into account the true technical scope of SPI for the skilled person.

Argument 2 : the SPI method comprising: providing one of the devices with the ability to tie the clock line to a potential representing a second logic value opposite the first logic value (Page 27, Figure 4-2, SCK=0 at SCK Edge Nr. 1); tying the clock line to the second logic value, via the one of the devices, after data is applied to the data line (Figure 4-2, Data

is applied before SCK Edge Nr. 1) ; and maintaining the data on the data line by the device sending the data (Figure 4-2, Data is applied until rising edge of clock) .

Applicants' comment: The Examiner has also considered that a change from the idle value to the active value is equivalent to a tying of the clock line, which is correct if it is admitted that the value defined by the polarization bit CPOL is equivalent to the default value of claim 1.

Argument 3: SPI does not specifically disclose maintaining the tie to the clock line by the device to which the data is sent and releasing the clock.

Applicants' comment: Agree with Examiner

Argument 4: However, SMB discloses maintaining the tie to the clock line by the device to which the data is sent (Page 22, Section 4.3.3, Figs. 4-7).

Applicants' comment: Agree with Examiner, but the value to which the clock line is tied corresponds to the period during which data are changed, as it will be developed below.

Argument 5: It would have been obvious to one of ordinary skill in the art to have the device receiving data to hold the clock down, as disclosed by SMB, in the method of SPI,

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Applicants' comment: from this point on, the Applicants respectfully submit that the reasoning of the Examiner is incorrect. Combining the teaching of SMB to SPI would mean that the skilled person would stretch the clock line when it has the idle value, and not the active value, since SMB teaches to stretch the clock outside the period of data validity (see FIG. 4.1.1 and FIG. 4.7 above), i.e., during the period when the change of data is allowed. This corresponds in the SPI bus to the period when the clock signal has the idle value.

Such an application of the SMB technique to the SPI would require that the slave is able to "tie" the clock line to the idle value, or rather to maintain it at the idle value. This does not make a lot of sense since it is assumed that the only value that can be tied is the active value opposite the default value (or "idle value" according to the Examiner).

In addition, even if it is it admitted that the skilled person would apply the SMB clock stretching technique to the SPI bus, the result of the combination of the two techniques would be a method different than that of the invention, that would be defined as follows (using the language of claim 1):

(SPI + SMB). A method of transmitting data between two devices via a clock line and at least one data line, the clock line being

maintained by default on a first logic value, the method comprising:

- providing each device with the ability to maintain the clock line to a potential representing the first value;
- providing one device ~~each device~~ with the ability to tie the clock line to a potential representing a second logic value opposite the first logic value;
- tying the clock line to the second logic value, with one ~~via the~~ devices, after data is applied to the data line; maintaining the tie to the clock line during a predetermined time ~~by the device to which the data is sent while the device has not read the data~~; and
- maintaining the data on the data line while the clock line is tied ~~by the device sending the data at least until an instant when the clock line is released by the device to which the data is sent~~,
- maintaining the clock line at the first logic value by the device receiving the data, to delay the sending of the next data.

Argument 6: this would allow clock synchronization to allow slower slave devices to cope with faster masters.

Applicants' comment: The Applicants agree that if this technique is implemented it would allow clock synchronization. However, in the event if it would allow clock synchronization, such a technique would be different from that of the invention.

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Argument 7: The combination of SPI and SMB would implicitly maintain data on the data line by the sending device until an instant after the slave releases the clock line since the data changes only on clock transitions in SPI and the clock only transitions when the slave release the clock in SMB.

Applicants' comment: This result cannot be obtained by combining SPI and SMB. This result is that of the invention. The Examiner has conducted an ex post facto reasoning and has not seriously considered what would be the combination of both techniques. Since SPI provides that the data are latched during transition of the clock, maintaining the clock when the data are valid would not provide more time to read the data.

In addition, combined teachings of SPI and SMB would not suggest features F4 and F5 of the invention, i.e.:

- The tie of the clock line is maintained by the device to which the data is sent while the device has not read the data,
- The data is maintained on the data line by the device sending the data at least until an instant when the clock line is released by the device to which the data is sent (i.e. until it knows, thanks to the release of the clock line, that the device has read the data).

In fact, these features which define the clock signal as a handshake signal cannot be present in the combined teachings

of SPI and SMB because both techniques do not use the clock signal as a handshake signal (in particular SPI teaches "sampling of data occurs at even edges of the SCK clock" or "sampling of data occurs at odd edges of the SCK clock" depending on the value of CPHA).

Therefore, even if SPI and SMB were combined, the result would be a system in which the device to which the data is sent never maintains the tie of the clock because it reads the data during the transition of the clock.

IV. CONCLUSION

The Examiner states that the combined teachings of SPI and SMB would have suggested that both a master and a slave device can tie a clock line to a second logic value opposite a first logic value.

However, in the method resulting from such combined teachings, what would be the function of the first logic value and of the second logic value in question, with respect to the data? In other words, would the "second logic value" - that the master and the salve both can tie - correspond to a validity period of the data or to the change of data period (or refresh of data period)?

Since SMB teaches to tie the clock during the change of data period, the second logic value should be the change of data period, and it should not be considered that the combined teachings of SPI and SMB would have suggested the invention.

The Applicants believe that the Examiner has erred in considering that the low value of the SMB clock signal corresponds to the active value of the SPI clock signal. The Examiner has merely

considered the electrical values of the clock signal (i.e. low) and not their function with respect to the transfer of data. The active value of the SPI clock signal is variable and depends upon the value of the polarization bit CPOL. Thus, the fact that the clock signal is low or high does not have any significance. Instead, the Examiner should have considered the value of the clock signal with respect to the data, i.e. a value corresponding to the data validity, and the value corresponding to the data change.

The Applicants submit that the Examiner has erred in considering that the combined teachings of SPI and SMB would suggest features F4 and F5 of the invention, i.e.:

- The tie of the clock line is maintained by the device to which the data is sent while the device has not read the data,
- The data is maintained on the data line by the device sending the data at least until an instant when the clock line is released by the device to which the data is sent (i.e. until it knows, thanks to the release of the clock line, that the other device has read the data).

As indicated above, these features which define the clock signal as a handshake signal cannot be present in the combined teachings of SPI and SMB because both techniques do not use the clock signal as a handshake signal (in particular SPI teaches "sampling of data occurs at even edges of the SCK clock" or "sampling of data occurs at odd edges of the SCK clock" depending on the value of CPHA). Therefore, even if SPI and SMB were combined, the result would be a system in which the device to which the data is sent never maintains the tie of the clock because it reads the data during the transition of the clock.

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In other respects, the Applicants do not believe that the slave must comply with a certain timeout is a good argument. In fact, a timeout may also be provided in the present invention, to prevent the slave from blocking the bus.

In view of the foregoing, it is submitted that all of the claims are patentable. Accordingly, a Notice of Allowance is respectfully requested in due course. Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,

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CERTIFICATE OF FACSIMILE TRANSMISSION

I HEREBY CERTIFY that the foregoing correspondence has been forwarded via facsimile number 571-273-8300 to the Commissioner for Patents on this 13 day of July, 2010.